SoLID DAQ preRD and plans

Data
Acquisition

SoLID collaboration meeting
June 22nd 2023

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- Outline

  - Capital
  - Testing
  - GEM chip
    - VMM
    - SALSA
    - APV25
  - Streaming DAQ

  - Conclusion

Capital equipement DAQ

Requested

Item	cost/item	number	total
FADC 250	6000	104	624000
Gigabit serial connectors			40000
Cables	100	1664	166400
VETROC	4000	30	120000
TD	3000	16	48000
VTP	10000	31	310000
SSP	5000	4	20000
VTP	8000	1	13000
TS	4000	1	4000
TID	3000	31	93000
SD	2500	32	80000
VXS crate	15000	32	480000
VME CPU	7000	32	224000
		Total	2217400
	FTE/year cost	months	
Syracuse	80000	12	80000
FEDAQ	120000	2	20000
Hall C	120000	2	20000
			2337400

Updated

Item	cost/item	number	total
FADC 250	6127	104	637208
Gigabit serial connectors	40000	1	40000
Cables	100	1664	166400
VETROC	4000	30	120000
TD	3000	16	48000
VTP	12500	31	387500
SSP	5000	4	20000
VTP	12500	1	12500
TS	4000	1	4000
TID	3000	31	93000
SD	2500	32	80000
VXS crate	19000	32	608000
VME CPU	9500	32	304000
		Total	2520608
	FTE/year cost	months	
Syracuse	67000	12	134000
FEDAQ	120000	2	20000
Hall C	120000	2	20000
			2694608

Testing

- SBS GEn
  - VTP readout
  - APV25
  - High data rate : 2.1 GB/s
- NPS
  - Calorimeter trigger
- SBS GEp
  - Calorimeter trigger
- HKS
  - Trigger with Cerenkov
  - High resolution TOF with MRPC
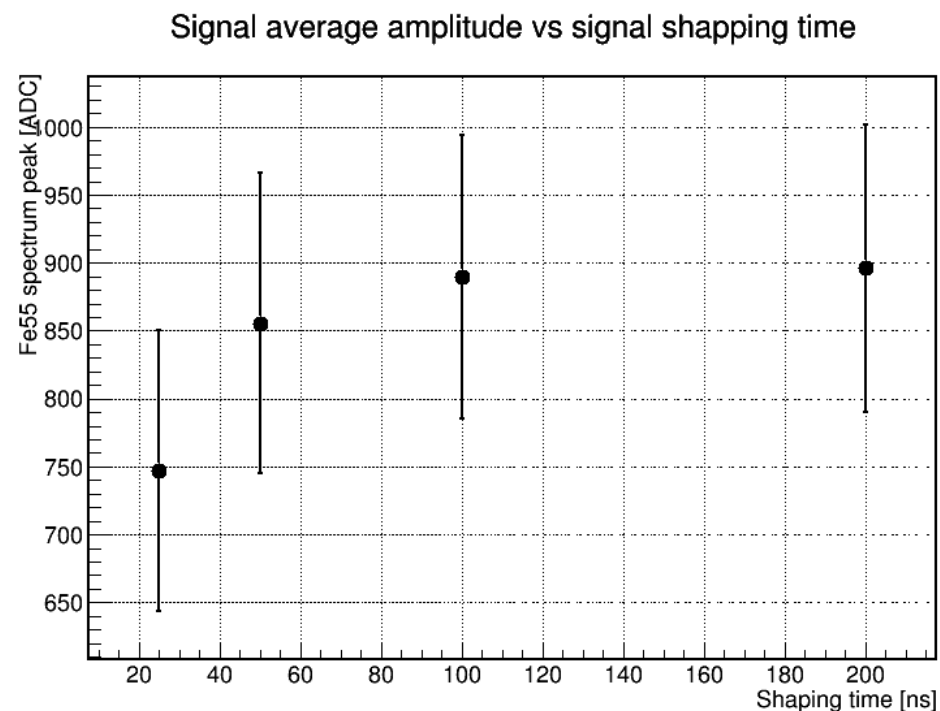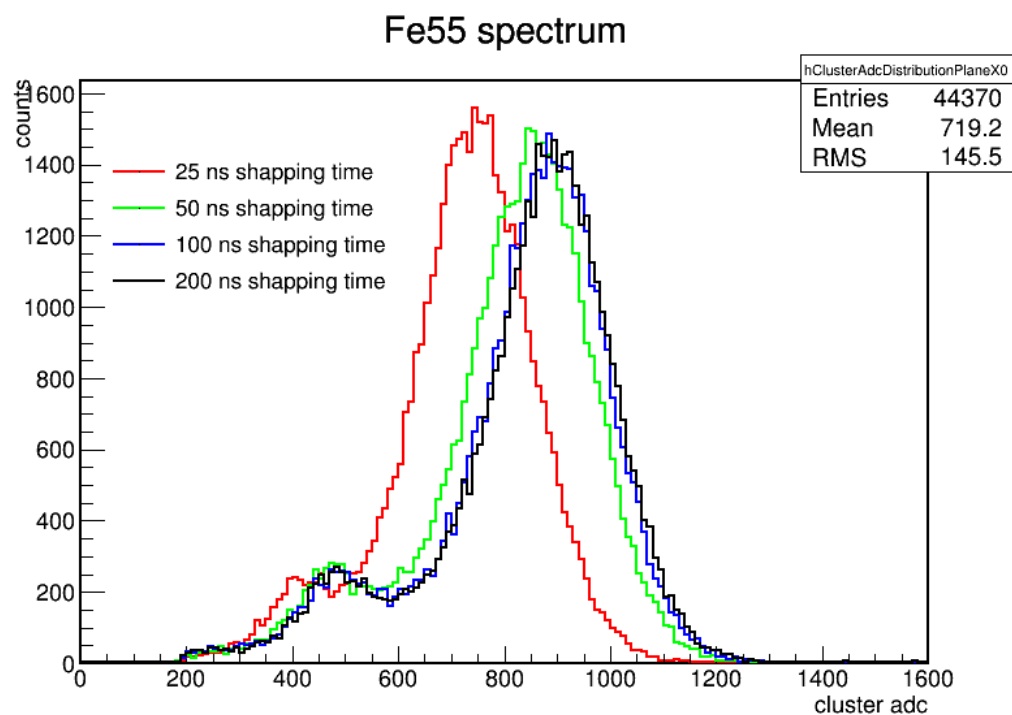- + parasitic beam tests

Future SoLID preRD

- Highest priority : GEM chip
  - Evaluate SALSA chip in high background environment
  - Improve VMM board signal to noise
  - Test with uRWell

- Calorimeter and Cerenkov readout
  - FADC ASIC to be placed on detector : only LV and optical fibers going out instead of BNC cables

- High resolution timing
  - AARDVARC test in beam
  - High resolution FADC timing ASICS

VMM test

- Ordered two test board 1500 $ x 2

- Build 6 SoLID prototype boards

- Evaluation board : can look at data with detector small subset of channels
  - Issue with external trigger but waiting for new firmware
  - Can check pedestal width
  - Signal to noise with detector with source and cosmics
  - Look at direct readout signals for 12 channels of detector

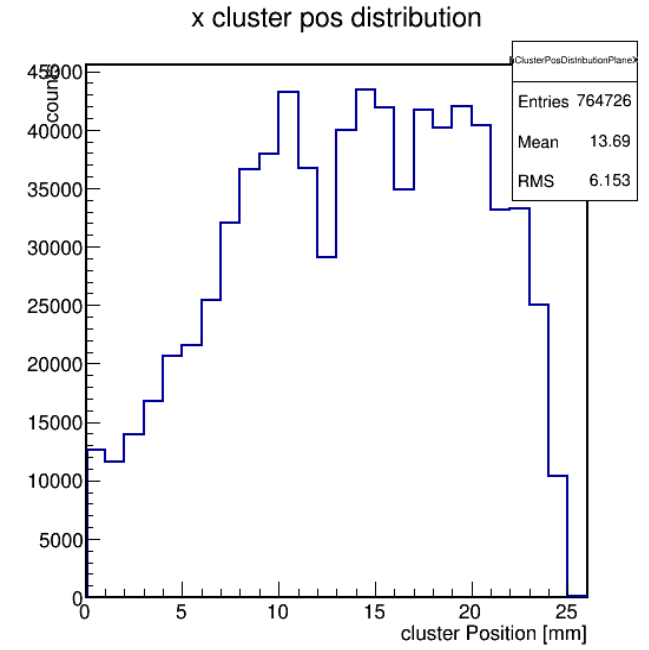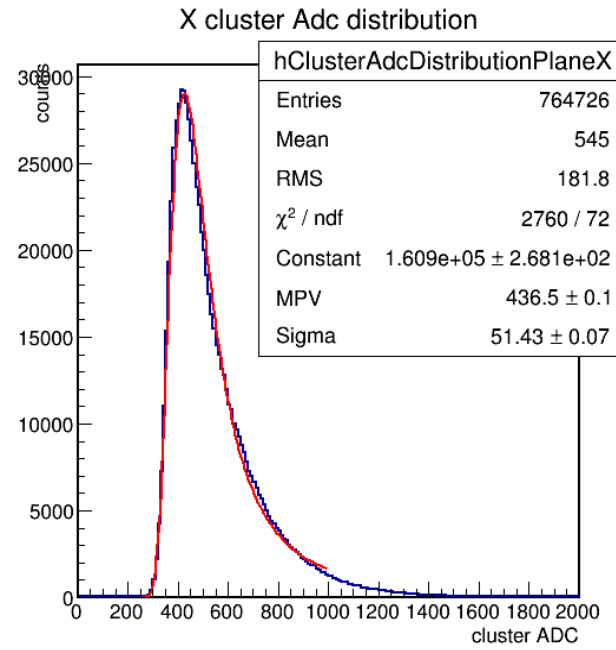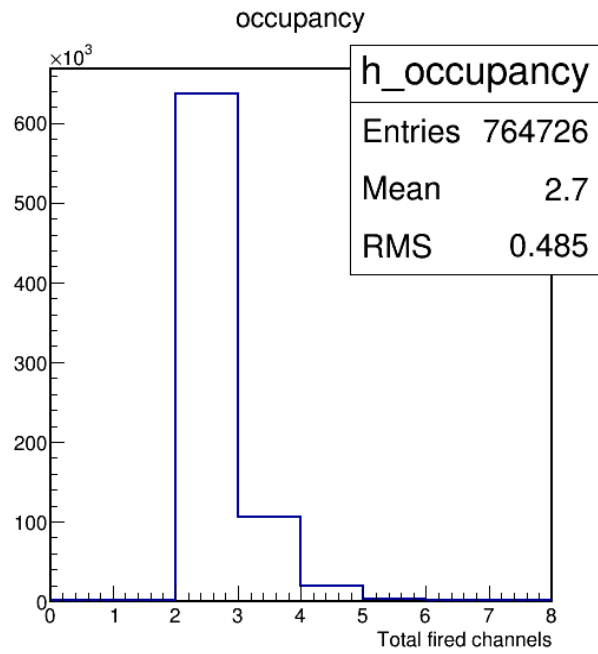- Prototype development for data performance, test direct output with detector and X-ray source

Signal gain vs shaping time, gain = 3 mV/fC

Fe55 spectrum

hClusterAdcDistributionPlaneX0	
Entries	44370
Mean	719.2
RMS	145.5

- 25 ns shapping time
- 50 ns shapping time
- 100 ns shapping time
- 200 ns shapping time

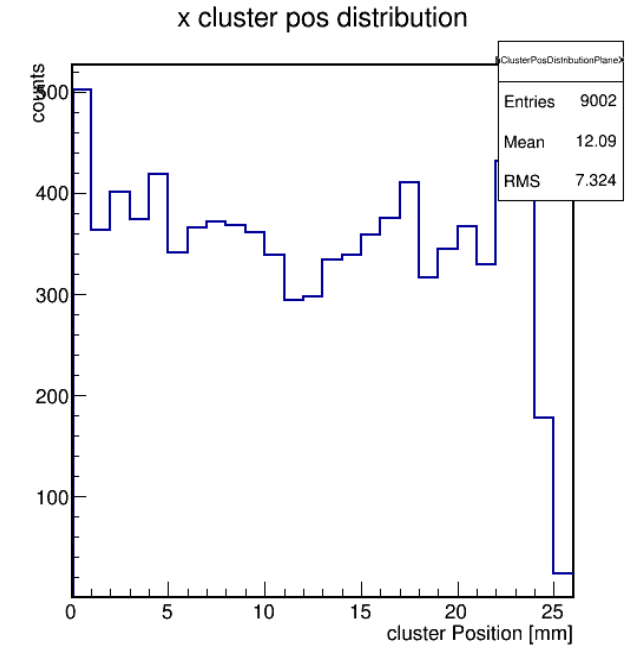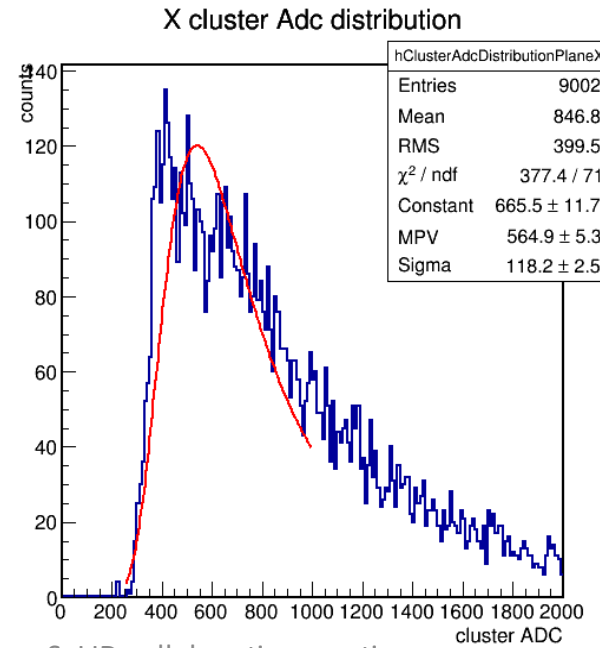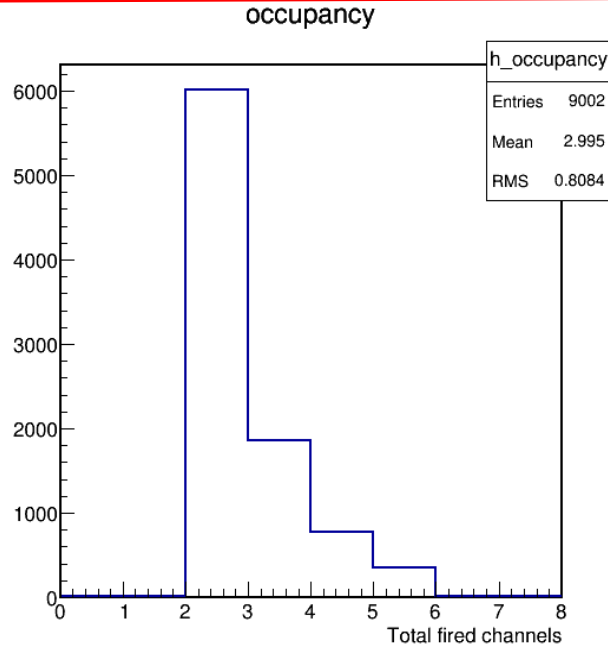Signal average amplitude vs signal shapping time

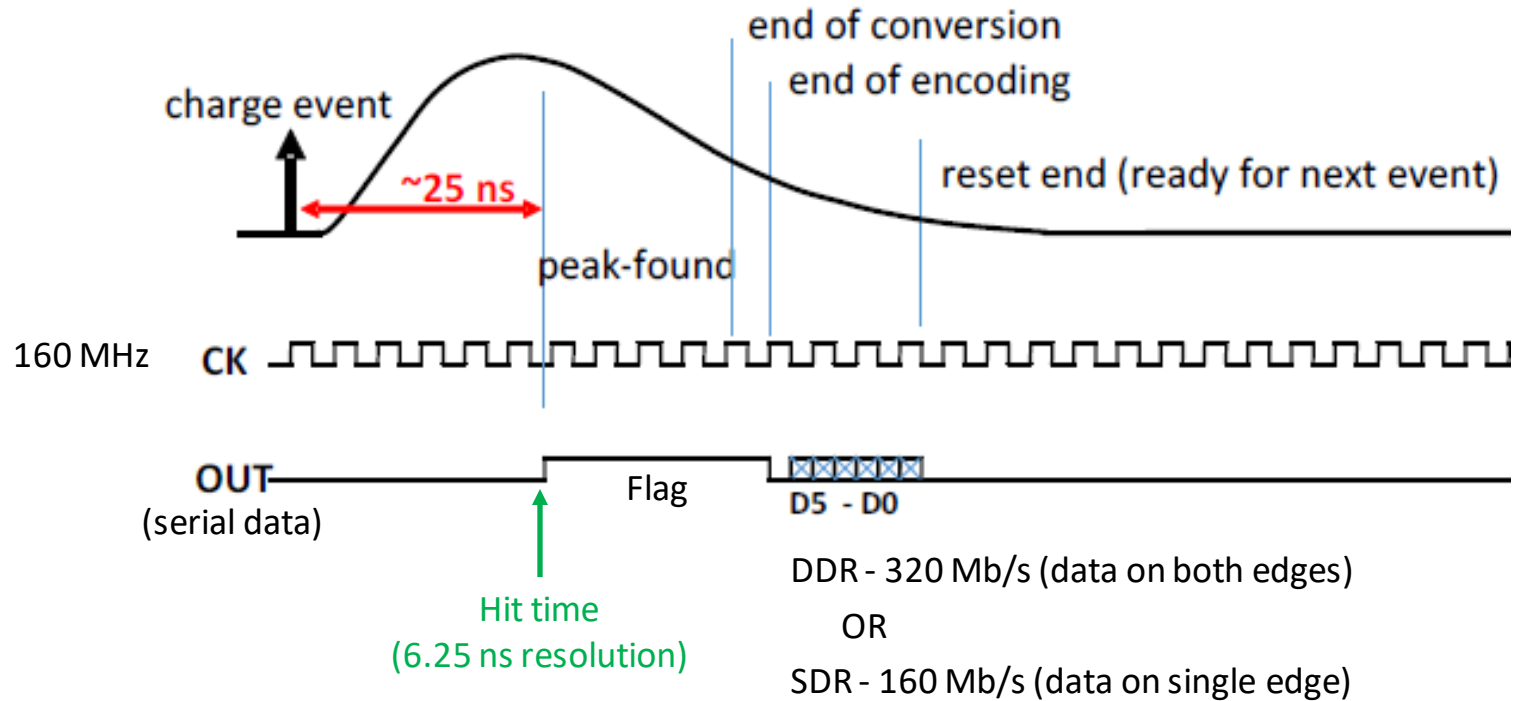From source data, 25 ns shaping only about 15 % lower than 50 ns, so 25 ns shaping useable

HV =

Sr90

Cosmic

128 channel VMM prototype for SoLID

- Features
  - Fast 6-bit ADC data from each channel allows for high hit rates (~10MHz/ch)
  - Dual readout paths (fiber)
    - 10GbE for low radiation environments (FPGA → SFP+)
    - Readout using CERN rad hard components (FPGA → GBTx → VTRx)
  - Power and signal interface through mezzanine cards
    - Initially use commercial components on mezzanines
    - Later mezzanines with rad hard components – <u>no modification of base board</u>
  - Mitigation of effects of radiation on FPGA by triplicating logic and adding voting circuitry (TMR)

  - Status
    - Commercial component mezzanine boards fabricated
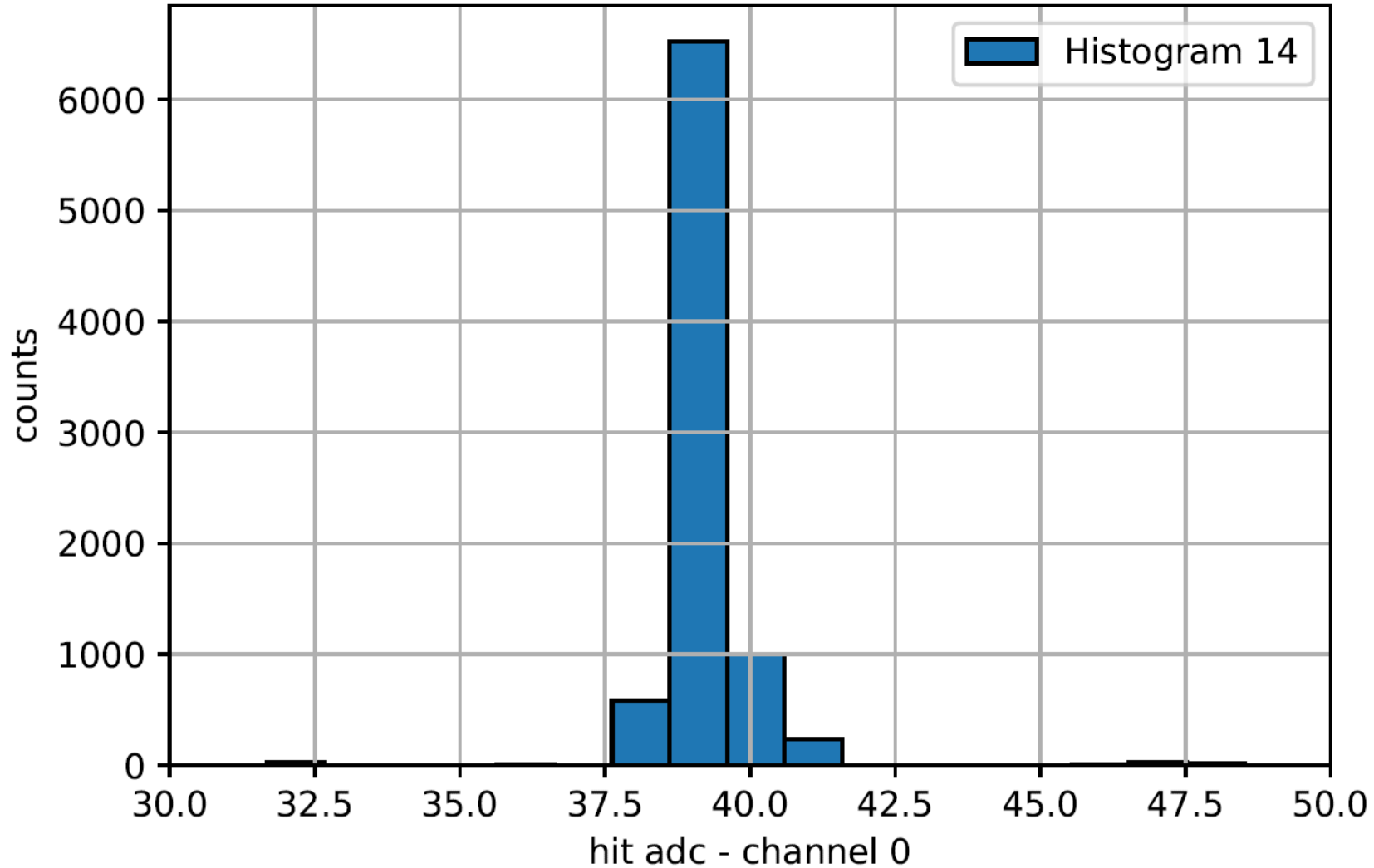   - Base board fabrication in early May

VMM 6-bit Direct Output data format

Peak amplitude converted to 6-bit value

charge event

~25 ns

end of conversion
end of encoding

reset end (ready for next event)

peak-found

160 MHz   CK

OUT
(serial data)

Flag

D5 - D0

Hit time
(6.25 ns resolution)

DDR - 320 Mb/s (data on both edges)

OR
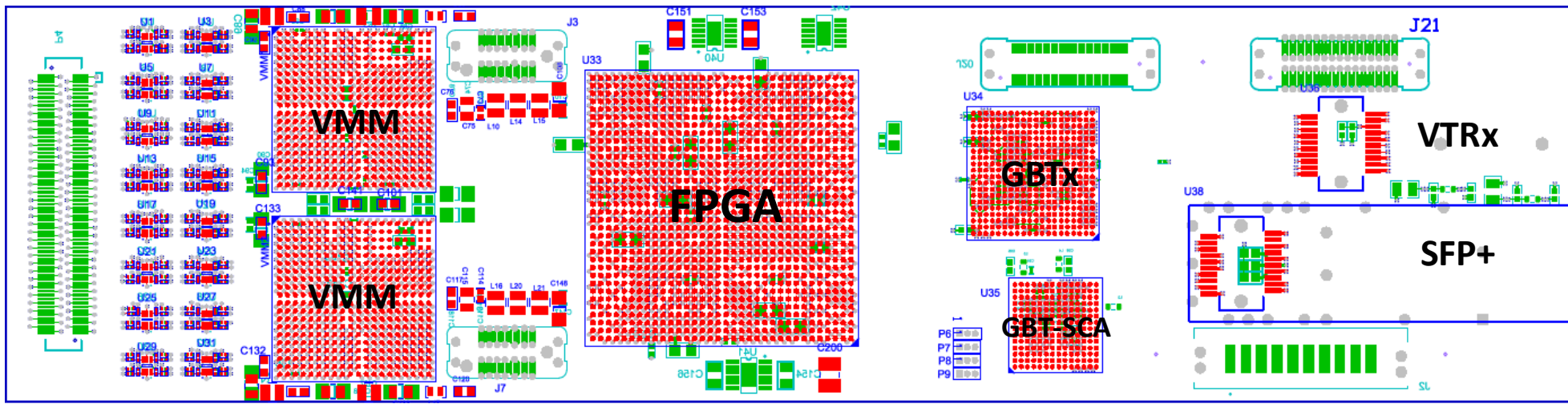
SDR - 160 Mb/s (data on single edge)

VMM 6-bit ADC direct data

(VMM evaluation board read out with Xilinx FPGA development card)

50mm

Base board

VMM

VMM

FPGA

GBTx

GBT-SCA

VTRx

SFP+

128 channel VMM prototype

VMM MEZZANINE PCB
FNAL JW 10/28/21
MADE IN THE U.S.A.

VMM power mezzanine

FPGA power mezzanine

| regulator | regulator | | regulator | regulator | regulator | regulator |

Connector to GEM

connector

board-to-board connectors
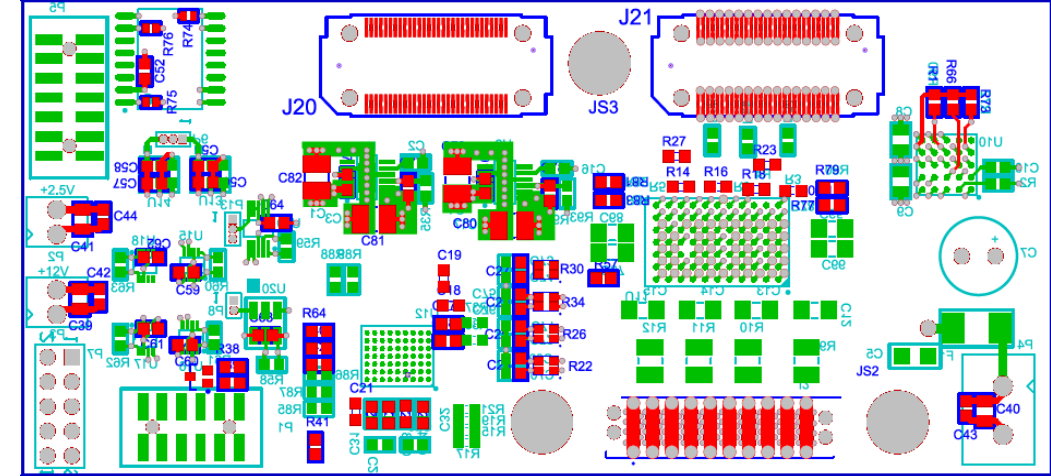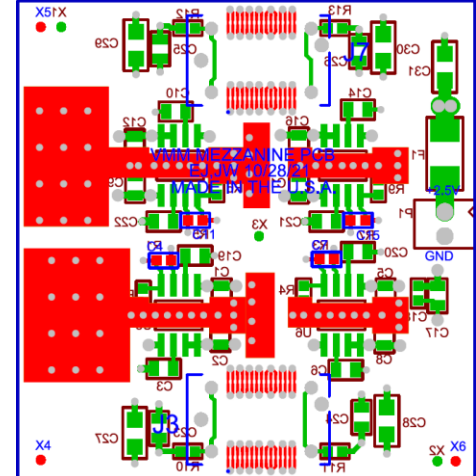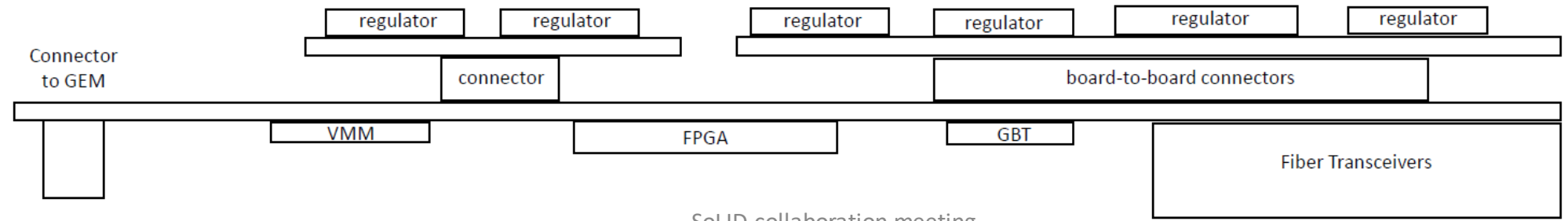
Assembly side view

VMM

FPGA

GBT

Fiber Transceivers

215mm

VMM dead time pulser test 6 bit

- Dead time is :

25 ns (peaking time)

+

5 ns (peak finding)

+

25 ns data conversion

+

7 x 6.25 ns data transfer

=

~120 ns

Can go down to ~ 90 ns when using DDR (6.25 / 2)
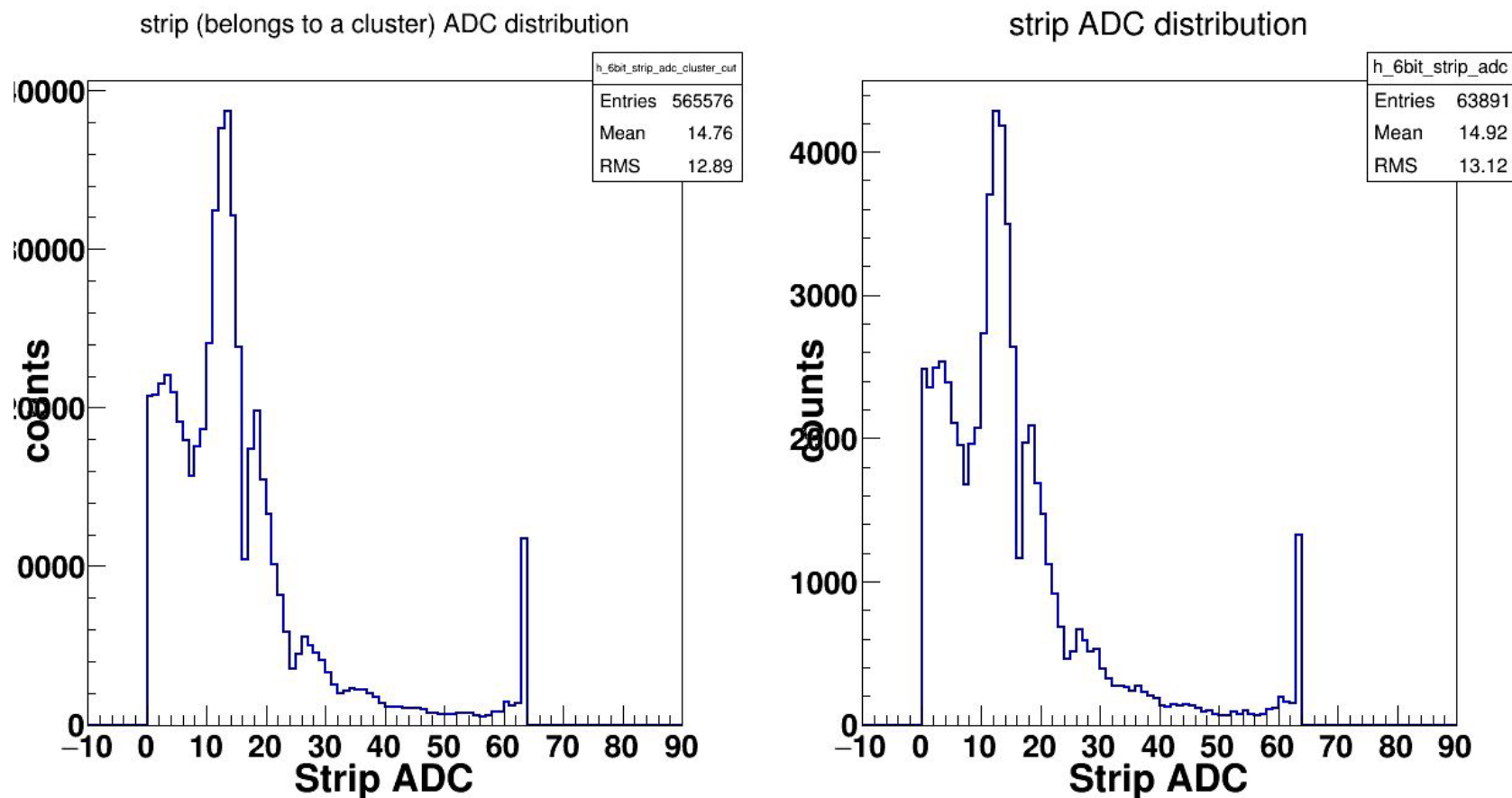
VMM dead time pulser test 10 bit

- Dead time is :

25 ns (peaking time)

+

5 ns (peak finding)

+

25 ns data conversion

+

7 x 6.25 ns data transfer

=

~120 ns

Can go down to ~ 90 ns when using DDR (6.25 / 2)

Sr90 VMM 6 bit 16mV/fC GEM at 4200 V

Noise 6 bit 16mV/fC Sr90
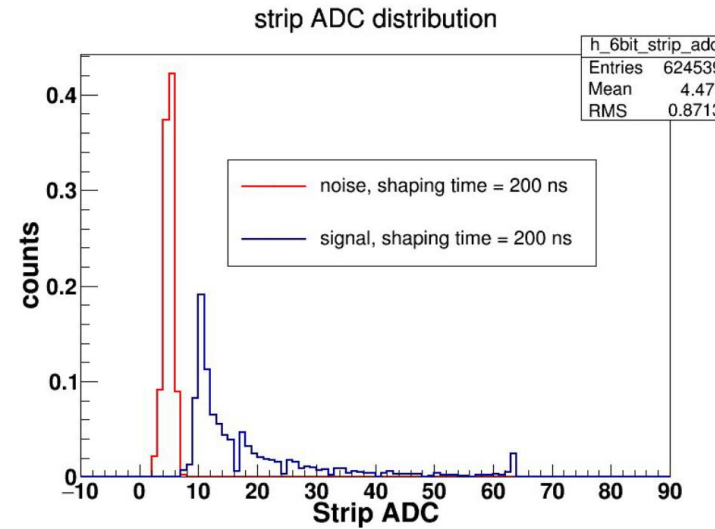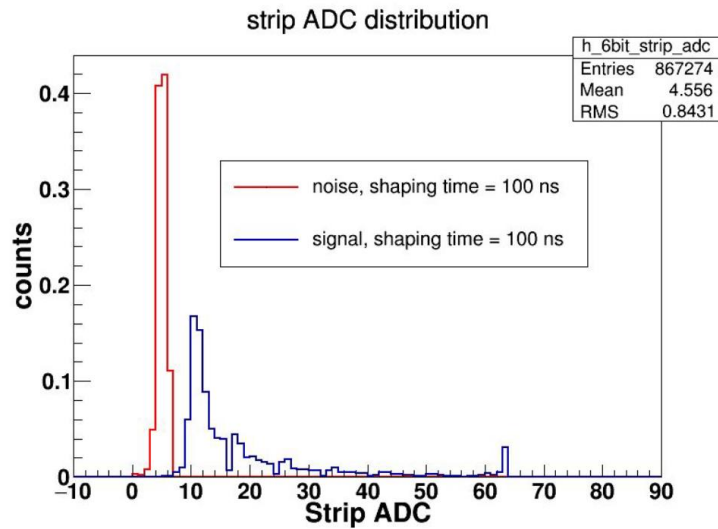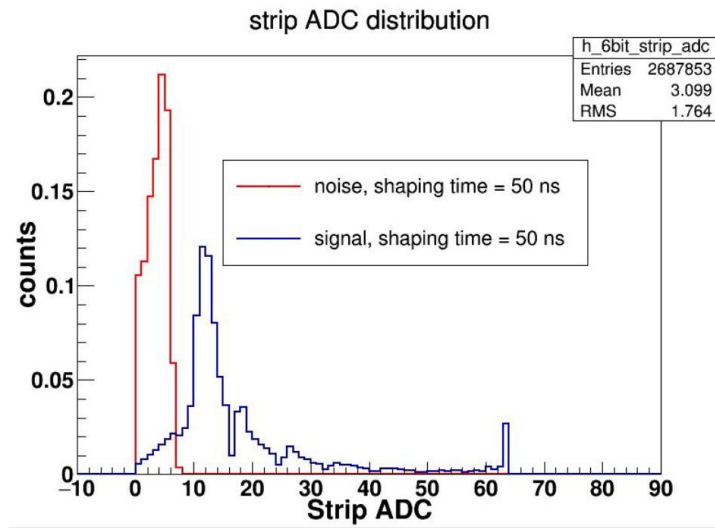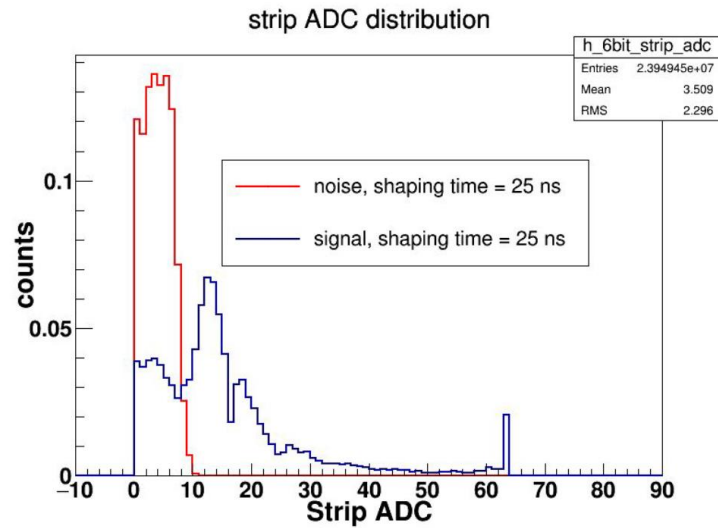
- Amplitude for MIP not change much
- Pedestal width dependent on peaking time

Conclusion VMM testing so far

- 90 ns dead time in 6 bit mode

- Some noise seen in prototype

- Noise larger with decreasing integration time

- MIP a bit low in dynamic range of 6 bit prototype

- Implementing 10 bit to cross compare with evaluation board

- 250 ns for 10 bit mode

- Implement higher gain : Compton preAMP maybe ? Or higher gain chip

- Would like to explore SALSA option : same performance as APV25 with no dead time

Streaming readout overview

Streaming readout

- Send all data from each detector continuously (or self triggered)
- Pro
  - No trigger
  - <u>If can be recorded : record all physics available</u>
  - If cannot be recorded : full reconstruction and record event of interest with advanced triggering or loose trigger
  - AIML algorithm very efficient with unbiased data samples
- Con
  - Need deadtime less electronics : ideally all FADCs (but high power comsuption)
  - Large amount of data to transfer to computer farm : cost in network
  - Large amount of data to be processed
  - Large amount of data to be recorded

Streaming readout option numbers

Detector	Area m2	SIDIS	Singles rate MHz	Event size bytes	Data rate GB	PVDIS	Singles rate MHz	Event size bytes	Data rate GB	JPSi	Singles rate MHz	Event size bytes	Data rate GB
LGC	0.7	16	112	16	1.792	80	560	88	49.28	40	280	16	4.48
HGC	1.2	160	1920	16	30.72		0	88	0		0	16	0
SPD_FA	15.2	0.02	3.04	16	0.04864		0	88	0	0.06	9.12	16	0.14592
SPD_LA	3.7	0.12	4.44	16	0.07104		0	88	0	0.25	9.25	16	0.148
EC_preshower_FA	19	33	6270	16	100.32	90	17100	88	1504.8	77	14630	16	234.08
EC_shower_FA	19	10	1900	16	30.4	9	1710	88	150.48	14	2660	16	42.56
EC_preshower_LA	4.1	45	1845	16	29.52		0	88	0	80	3280	16	52.48
EC_preshower_LA	4.1	5	205	16	3.28		0	88	0	19	779	16	12.464
GEM	37	800	296000	16	4736	500	185000	16	2960	1600	592000	16	9472
	Rate in GB/s				4932				4664				9818

Around 10 to 5 TB/s, about 1000 more data than triggered

AI/ML hardware acceleration

Type	Hardware	Inference time	Max throughput (img/s)	Setup
CPU	Xeon 2.6 GHz,1 core	1.75 s	0.6	CMSSW, TF v1.06
CPU	i7 3.6 GHz,1 core	500 ms	2	python, TF v1.10
CPU	i7 3.6 GHz,8 core	200ms	5	python, TF v1.10
GPU (batch=1)	NVidia GTX 1080	100 ms	10	python, TF v1.10
GPU (batch=32)	NVidia GTX 1080	9 ms	111	python, TF v1.10
GPU (batch=1)	NVidia GTX 1080	7 ms	143	TF internal TF v1.10
GPU (batch=32)	NVidia GTX 1080	1.5 ms	667	TF internal TF v1.10
Brainwave	Altera Artix	10 ms	660	CMSSW, on-prem
Brainwave	Altera Artix	60 ms	660	CMSSW, remote

Could gain factor of ~ 100 processing with GPUs, might be able to do better

Salsa

- Collaboration of Irfu CEA Saclay and U. of Sao Paulo.
- SALSA

- 64-Ch, updated design from SAMPA V5, migrating to 65 nm CMOS.
- Peaking time: 50 – 500 ns
- Inputs: Cin optimized for 200 pF; Rates: 25 kHz/Ch; Dual polarity.
- ADC: 12 bits, 10 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Gbps links.
- I2C configuration.

- Evaluation board available this year - Might want a dedicated SoLID version to match tracker low gain operation and handle high rates at input

- Conclusion

  - Capital equipment
    - All elements for SoLID DAQ besides CPU procured

  - Developments of SoLID trigger and readout in previous and upcoming experiments

  - ASICs development could benefit SoLID

  - GEM chip solution to be finalized
    - VMM can work but not ideal
    - SALSA promising but need R&D for high rate operation
    - APV25 readout update can be fall back for 100 k channels

  - Streaming option
    - About 5 to 10 TB/s about 1000 more than triggered
    - Might be able to handle with AIML progress, network progress and CPU
    - Streaming readout is an option with upgrade of data links and HPDF

  - SoLID in streaming mode, could be the ultimate JLab detector – Just run detector at full luminosity all the time and extract all possible physics after the run